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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,985	07/25/2001	Detlef Hommel	1999P8006 US N	8172

7590 02/27/2004

LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/915,985	Applicant(s) HOMMEL ET AL.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>December 12, 2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Shimizu et al (US 5998925), hereafter Shimizu in view of Hide et al. (US 9633393), hereafter Hide.

Regarding claim 1, Fig. 2 of Shimizu shows an electroluminescent semiconductor device for comprising:

a semiconductor chip having a first layer (201; a phosphor layer) and a second semiconductor layer (202) adjacent to the first layer;

the second semiconductor layer including an electroluminescent region emitting visible light of a first color (blue) having a first wavelength (abstract; col.10, lines 2-5);

the first layer absorbing part of the visible light of the first color and the first layer re-emitting visible light of a second color (yellow) having a second wavelength, the second color being different from the first color, and the second wavelength being longer than the first wavelength (abstract; col.10, lines 2-5);

the semiconductor chip emitting the visible light of the second color together with the visible light of the first color.

Shimizu fails to teach that the first layer is a semiconductor layer. Hide discloses that a phosphor layer formed on the adjacent light emitting layer can be made of

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semiconductor material such as ZnS and ZnCdS. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ the teaching of Hide to the first layer of Shimizu's device to be made of semiconductor layer for reduction of a manufacturing process.

Also, it would be obvious for the first layer is in allowed energy level since the first layer of Shimizu absorbs the part of the emitted light from the light emitting layer (202) and re-emits a second color (yellow) as identically recited in the pending claim.

Regarding claim 4, it is inherent that the device with the combined teachings of Shimizu and Hide has a substrate.

Note that "epitaxially grown" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985), and a limitation of "is also utilized" designates for intended use which does not carry patentable weight in device claims.

Regarding claim 8, Fig.4 of Hide shows that semiconductor chip being disposed in a parabolic mirror (16).

Regarding claim 9, Shimizu shows the first layer and second semiconductor layer are configured to emit white light from the semiconductor chip (abstract).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu and Hide as applied to claim 1 above, and further in view of Kitagawa et al. (US 5198690), hereafter Kitagawa.

Regarding claim 5, the combined teachings of Shimizu and Hide show substantially an entire claimed structure except "the semiconductor chip includes a

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growth substrate and the first semiconductor layer is disposed between the growth substrate and the second semiconductor layer.” Kitagawa shows a semiconductor chip includes a growth substrate and the first semiconductor layer is disposed between the growth substrate and the second semiconductor layer (col. 12, lines 8-14). It would have been obvious to one of ordinary skill in the art at the time of the invention was to utilize the teachings of Kitagawa into the device of Shimizu and Hide in order to have a growth substrate under the first layer for an intended process need.

Regarding claim 6, the combined teachings of Shimizu and Hide show substantially an entire claimed structure except “a semiconductor chip includes a growth substrate for epitaxially growing the second semiconductor layer and the second semiconductor layer has a side opposite the growth substrate while the first semiconductor layer is disposed on the side of the second semiconductor layer opposite said growth substrate.” Kitagawa shows a semiconductor chip includes a growth substrate for epitaxially growing the second semiconductor layer and the second semiconductor layer has a side opposite the growth substrate while the first semiconductor layer is disposed on the side of the second semiconductor layer opposite said growth substrate (col. 12, lines 8-16). It would have been obvious to one of ordinary skill in the art at the time of the invention was to utilize the teachings of Kitagawa into the device of Shimizu and Hide in order to have a growth substrate under the first layer for a desired device configuration.

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Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu and Hide as applied to claim 1 above, and further in view of Henry et al. (US 4,570,172), hereafter Henry.

Regarding claim 3, the combined teachings of Shimizu and Hide show substantially an entire claimed structure except the first layer includes a material with an absorption edge having an energy level corresponding to a third wavelength which is longer than the first wavelength of the visible light emitted by the semiconductor layer and is shorter than the second wavelength and re-emitting radiation of the second wavelength when excited with radiation of a wavelength shorter than the third wavelength. Henry shows a wavelength of a light emitted from re-emitting layer (7) in Fig. 5 is longer than a wavelength of a light emitted from the first layer and shorter than a wavelength of a light emitted from the second layer with the claimed emission state. (col. 4, lines 47-68). It would have been obvious to one of ordinary skill in the art at the time of the invention was to incorporate the teaching of Henry into the device taught by Kimizu and Hide since such a layer minimizes the possible migration defects of the light in the substrate.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu and Hide as applied to claim 1 above, and further in view of Ishikawa et al. (US 5,488,233), hereafter Ishigawa.

Regarding claim 7, the combined teachings of Kimizu and Hide fail to teach the that the first semiconductor layer includes doped ZnSe and the second semiconductor layer has an active zone containing $\text{Cd}_x\text{Zn}_{1-x}\text{Se}/\text{ZnSe}$ with $0 \leq x \leq 1$. Ishikawa shows that

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an LED with a CdZnSe/ZnSe layer (107) in Fig.5, formed between the light emitting layers. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ the teaching of Ishikawa to the device taught by Kimizu and Hide since such modification can improve reliability of the device with better light emitting efficiency.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jmi
February 5, 2004



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800